AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A method of implementing a design in a programmable logic device (PLD) to reduce susceptibility to single-event upsets (SEUs), the design comprising source logic, destination logic, and a node coupled between the source logic and the destination logic, the method comprising:

assigning the source logic to a first logic block in the PLD;

assigning the destination logic to a second logic block in the PLD;

identifying first and second data input terminals of a programmable routing multiplexer in the PLD, wherein a selection between the first and second data input terminals is determined solely by a first value stored in a first memory cell controlling the programmable routing multiplexer;

routing the node on a first routing path between the first and second logic blocks, wherein the first routing path traverses the programmable routing multiplexer via the first data input terminal; and

routing the node on a second routing path between the first and second logic blocks, wherein the second routing path traverses the programmable routing multiplexer via the second data input terminal.

2. (Currently Amended) The method of Claim 1, further comprising:

identifying a third data input terminal of the programmable routing multiplexer, wherein a selection between the first and third data input terminals is determined solely by a second value stored in a second memory cell controlling the programmable routing multiplexer; and

routing the node on a third routing path between the first and second logic blocks, wherein the third routing path traverses the programmable routing multiplexer via the third data input terminal.

3. (Original) The method of Claim 1, wherein the PLD is a field programmable gate array (FPGA).

4. (Original) The method of Claim 3, wherein the first memory cell is a static RAM-based configuration memory cell of the FPGA.

5. (Original) The method of Claim 1, wherein the multiplexer is a 4-to-1 multiplexer.

6. (Original) The method of Claim 1, wherein the identifying, the routing the node on the first routing path, and the routing the node on the second routing path are performed interactively with each other.

7. (Original) The method of Claim 1, further comprising:

evaluating the source and destination logic and determining that the source and destination logic do not form a portion of a triple modular redundancy (TMR) circuit.

8. (Currently Amended) A computer-readable storage medium comprising computer-executable code for implementing a design in a programmable logic device (PLD) to reduce susceptibility to single-event upsets (SEUs), the design comprising source logic, destination logic, and a node coupled between the source logic and the destination logic, the medium comprising:

code for assigning the source logic to a first logic block in the PLD and assigning the destination logic to a second logic block in the PLD; and

code for:

identifying first and second data input terminals of a programmable routing multiplexer in the PLD, wherein a selection between the first and second data input terminals is determined solely by a value stored in a memory cell controlling the programmable routing multiplexer,

routing the node on a first routing path between the first and second logic blocks, wherein the first routing path traverses the programmable routing multiplexer via the first data input terminal, and

routing the node on a second routing path between the first and second logic blocks, wherein the second routing path traverses the programmable routing multiplexer via the second data input terminal.

9. (Original) The computer-readable storage medium of Claim 8, further comprising code for evaluating the source and destination logic and determining that the source and destination logic do not form a portion of a triple modular redundancy (TMR) circuit.

10. (Currently Amended) A computer system for implementing a design in a programmable logic device (PLD) to reduce susceptibility to single-event upsets (SEUs), the design comprising source logic, destination logic, and a node coupled between the source logic and the destination logic, the computer system comprising:

a placement module for assigning the source logic to a first logic block in the PLD and assigning the destination logic to a second logic block in the PLD; and

a routing module for:

identifying first and second data input terminals of a programmable routing multiplexer in the PLD, wherein a selection between the first and second data input terminals is determined solely by a value stored in a memory cell controlling the programmable routing multiplexer;

routing the node on a first routing path between the first and second logic blocks, wherein the first routing path traverses the programmable routing multiplexer via the first data input terminal; and

routing the node on a second routing path between the first and second logic blocks, wherein the second routing path traverses the programmable routing multiplexer via the second data input terminal.

11. (Original) The computer system of Claim 10, further comprising an evaluation module for evaluating the source and destination logic and determining that the source and destination logic do not form a portion of a triple modular redundancy (TMR) circuit.

12. (Currently Amended) A method of implementing a design in a programmable logic device (PLD) to reduce susceptibility to single-event upsets (SEUs), the design comprising source logic, destination logic, and a node coupled between the source logic and the destination logic, the method comprising:

generating a PLD placement wherein the source logic is assigned to a first logic block in the PLD and the destination logic is assigned to a second logic block in the PLD;

routing the PLD placement to generate a routed design wherein the node is routed on a first routing path between the first and second logic blocks, the first routing path traversing a programmable routing multiplexer via a first data input terminal of the programmable routing multiplexer;

identifying a second data input terminal of the programmable routing multiplexer, wherein a selection between the first and second data input terminals is determined solely by a first value stored in a first memory cell controlling the programmable routing multiplexer; and

routing the node on a second routing path between the first and second logic blocks, wherein the second routing path traverses the programmable routing multiplexer via the second data input terminal.

13. (Currently Amended) The method of Claim 12, further comprising:

identifying a third data input terminal of the programmable routing multiplexer, wherein a selection between the first and third data input terminals is determined solely by a second value stored in a second memory cell controlling the programmable routing multiplexer; and

routing the node on a third routing path between the first and second logic blocks, wherein the third routing path traverses the programmable routing multiplexer via the third data input terminal.

14. (Original) The method of Claim 12, wherein the PLD is a field programmable gate array (FPGA).

15. (Original) The method of Claim 14, wherein the first memory cell is a static RAM-based configuration memory cell of the FPGA.

16. (Original) The method of Claim 12, wherein the multiplexer is a 4-to-1 multiplexer.

17. (Original) The method of Claim 12, further comprising:

evaluating the node and determining that the node is not included in a triple modular redundancy (TMR) circuit.

18. (Withdrawn) A computer-readable storage medium comprising computer-executable code for implementing a design in a programmable logic device (PLD) to reduce susceptibility to single-event upsets (SEUs), the design comprising source logic, destination logic, and a node coupled between the source logic and the destination logic, the medium comprising:

code for generating a PLD placement wherein the source logic is assigned to a first logic block in the PLD and the destination logic to a second logic block in the PLD;

code for routing the PLD placement to generate a routed design wherein the node is routed on a first routing path between the first and second logic blocks, the first routing path traversing a programmable routing multiplexer via a first data input terminal of the programmable routing multiplexer; and

code for performing post-processing of the routed design, comprising:

code for identifying a second data input terminal of the programmable routing multiplexer, wherein a selection between the first and second data input terminals is determined by a value stored in a memory cell controlling the programmable routing multiplexer, and

code for routing the node on a second routing path between the first and second logic blocks, wherein the second routing path traverses the programmable routing multiplexer via the second data input terminal.

19. (Withdrawn) The computer-readable storage medium of Claim 18, further comprising code for evaluating the node and determining that the node is not included in a triple modular redundancy (TMR) circuit.

20. (Withdrawn) A computer system for implementing a design in a programmable logic device (PLD) to reduce susceptibility to single-event upsets (SEUs), the design comprising source logic, destination logic, and a node coupled between the source logic and the destination logic, the computer system comprising:

a placement module for generating a PLD placement wherein the source logic is assigned to a first logic block in the PLD and the destination logic to a second logic block in the PLD;

a routing module for routing the PLD placement to generate a routed design wherein the node is routed on a first routing path between the first and second logic blocks, the first routing path traversing a programmable routing multiplexer via a first data input terminal of the programmable routing multiplexer; and

a post-processing module for:

identifying a second data input terminal of the programmable routing multiplexer, wherein a selection between the first and second data input terminals is determined by a value stored in a memory cell controlling the programmable routing multiplexer; and

routing the node on a second routing path between the first and second logic blocks, wherein the second routing path traverses the programmable routing multiplexer via the second data input terminal.

21. (Withdrawn) The computer system of Claim 20, further comprising an evaluation module for evaluating the node and determining that the node is not included in a triple modular redundancy (TMR) circuit.

22. (Currently Amended) A method of implementing a design in a programmable logic device (PLD) to reduce susceptibility to single-event upsets (SEUs), the method comprising:

identifying in a programmable routing multiplexer of the PLD a first data input terminal and a second data input terminal, wherein a selection between the first and second data input terminals is determined solely by a first value stored in a first memory cell controlling the programmable routing multiplexer;

routing a node in the design to the first data input terminal; and

routing the node to the second data input terminal.

23. (Currently Amended) The method of Claim 22, further comprising:

identifying in the programmable routing multiplexer a third data input terminal, wherein a selection between the first and third data input terminals is determined solely by a second value stored in a second memory cell controlling the programmable routing multiplexer; and

routing the node to the third data input terminal.

24. (Original) The method of Claim 22, wherein the PLD is a field programmable gate array (FPGA).

25. (Original) The method of Claim 24, wherein the first and second memory cells are static RAM-based configuration memory cell of the FPGA.

26. (Original) The method of Claim 22, wherein the multiplexer is a 4-to-1 multiplexer.

27. (Original) The method of Claim 22, further comprising:

evaluating the node and determining that the node is not included in a triple modular redundancy (TMR) circuit.

28. (Currently Amended) A computer-readable storage medium comprising computer-executable code for implementing a design in a programmable logic device (PLD) to reduce susceptibility to single-event upsets (SEUs), the medium comprising:

code for identifying in a programmable routing multiplexer of the PLD a first data input terminal and a second data input terminal, wherein a selection between the first and second data input terminals is determined solely by a first value stored in a first memory cell controlling the programmable routing multiplexer; and

code for routing a node in the design to both of the first and second data input terminals.

29. (Original) The computer-readable storage medium of Claim 28, further comprising code for evaluating the node and determining that the node is not included in a triple modular redundancy (TMR) circuit.

30. (Currently Amended) A computer system for implementing a design in a programmable logic device (PLD) to reduce susceptibility to single-event upsets (SEUs), the computer system comprising:

an identification module for identifying in a programmable routing multiplexer of the PLD a first data input terminal and a second data input terminal, wherein a selection between the first and second data input terminals is determined solely by a first value stored in a first memory cell controlling the programmable routing multiplexer; and

a routing module for routing a node in the design to both of the first and second data input terminals.

31. (Original) The computer system of Claim 30, further comprising an evaluation module for evaluating the node and determining that the node is not included in a triple modular redundancy (TMR) circuit.